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09/527,343	03/17/2000	Timothy E. Giorgetta	AMCC4100	3311

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EXAMINER
WILSON, ROBERT W

ART UNIT	PAPER NUMBER
2661	4

DATE MAILED: 08/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/527,343	GIORGETTA ET AL.	
	Examiner	Art Unit	
	Robert W Wilson	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☒ Claim(s) *7-11,15 and 23-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1.0 The application of Timothy E. Giorgetta et al. for "Transposable Frame Synchronization Structure" filed 3/17/2000 without a foreign priority has been examined. Claims 1-31 are pending.

Drawings

2.0 The drawings were accepted by the draftsperson as formal.

Claim Objections

3.0 Claims 7-11, 15, and 23-25 are objected to because of the following informalities: The word "stream" is misspelled as "steam" for example in Claims 7, 9, 23, and 25. There are two claims 15. It should be noted that the examiner refers two the two Claim 15s as Claim 15A and 15B in the rejection. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.0 Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over SONET 101

Referring to claim 1, SONET 101 teaches: A method for varying the frame synchronization structure of an information stream (Fig 1-9), the method comprising; Receiving a first stream of information (data into Service Adapters per Fig 1-2);

Selecting a first arrangement of synchronization bits (The Service Adapters per Fig 1-2 take the DS-3 first stream and organize the DS-3 into the STS-1 or SPE with pointers which are the synchronization bits in the SONET FRAME or first frame structure per Fig 1-2, 1-7, and 1-9).

In response to selecting the first arrangement of synchronization bits, synchronization the first information stream into a first frame structure (The Service Adapters per Fig 1-2 take the DS-3 first stream and organize the DS-3 into the STS-1 or SPE with pointers which are the synchronization bits in the SONET FRAME or first frame structure per Fig 1-2, 1-7, and 1-9).

In Addition:

Reading the first arrangement of synchronization bits in the first stream of information; and in response to reading the first arrangement of synchronization bits, organizing the first information stream into header and data sections (The Service Adapters per Fig 1-2 take the DS-3 or first stream and organize the SONET FRAME FORMAT into a STS-1 or SPE with pointers which are the synchronization bits in the SONET FRAME or first frame structure per Fig 1-2, 1-7, and 1-9) as claimed in **Claim 2.**

In which the selection of the first arrangement of synchronization bits includes selecting a first arrangement of bits in the header section (The pointer or synchronization bits defines the location of the STS-1 or SPE per Fig 1-9) as claimed in **Claim 3.**

In which the organization of the first information stream into the first frame structure of header and data sections includes each header section having a plurality of m bits (Organization of the DS-3 per Fig 1-2 into an STS-1 or SPE per Fig 1-9 has a SONET header and SONET data section with a plurality of m bits);
And in which the selection of the first arrangement of synchronization bits includes selecting a number of bits in the range from zero to m bits in the header section (The pointer or synchronization bits in the header consists of zero to m bits per Figs 1-9) as claimed in **Claim 4.**

Which the selection of the first arrangement of synchronization bits includes selecting the bit position of each synchronization bit in the header (The pointers or synchronization bits are selected from specific bit positions in the SONET header per Fig 1-9) as claimed in **Claim 5.**

In which the selection of the first arrangement of synchronization bits includes selecting the contents of the bits in the selected bit positions in the header section (The pointers or synchronization bits are selected from specific bit positions in the SONET header per Fig 1-9) as claimed in **Claim 6**

Deinterleaving the first stream of information into a plurality of n parallel data streams (DS-1s per Fig 1-2 are in n parallel streams)
In which the organization of the first stream of information into the first frame structure includes each parallel data stream having a header and a data section (The DS-1s are organized into VTs per Fig 1-7); and

In which the selection of the first arrangement of synchronization bits, one arrangement for each parallel data stream header section (It would be obvious to one of ordinary skill in the art at the time of the invention that the VTs have pointers or synchronization bits in the header associated with each stream per Figs 1-2, 1-7, and 1-9) as claimed in **Claim 7.**

In which the selection of the first arrangement of synchronization bits in the header sections of the n parallel data streams includes selecting a unique arrangement of synchronization for each parallel data stream header section (It would be obvious to one of ordinary skill in the art at the time of the invention that the VTs have pointers or synchronization bits which point out where each of the parallel streams is carried in the SONET frame per Figs 1-2, 1-7, and 1-9) as claimed in **Claim 8.**

In which the deinterleaving of the first stream of digital information includes forming four parallel data streams (It would be obvious to one of ordinary skill in the art at the time of the invention that the DS-1s per Fig 12 are formed into VTs per Fig Fig 1-7); and

In which the reading of synchronization bits from the header sections of the parallel data streams includes reading a first group of synchronization bits from the first parallel data stream header section, a second group of synchronization bits from the second parallel data stream header, a third group of synchronization bits from the third parallel data stream header section, and a fourth group of synchronization bits from the fourth parallel data stream header section((It would be obvious to one of ordinary skill in the art at the time of the invention that there are pointer bits in the SONET frame which point to the VTS per Figs 1-2, 1-7, and 1-9 associated with Groups 1-4) as claimed in **Claim 9**

In which the selection of the first arrangement of overhead bits includes:
selecting a bit position for each of the first group of bits in the first header (Pointer for first VT per Figs 1-2, 1-7, and 1-9)

selecting a bit position for each of the second group of bits in the second header section (Pointer for second VT per Figs 1-2, 1-7, and 1-9)

selecting a bit position for each of the third group of bits in the third header section (Pointer for third VT per Figs 1-2, 1-7, and 1-9)
selecting a bit position for each of the fourth group of bits in the fourth header (Pointer for the fourth VT per Figs 1-2, 1-7, and 1-9) as claimed in **Claim 10.**

In which the selection of the first arrangement of synchronization bits includes selecting the number of synchronization bits in the first, second, third, and fourth groups of synchronization bits (Pointer or synchronization bits in the header for the first-fourth VTs per Figs 1-2, 1-7, and 1-9) as claimed in **Claim 11**.

Organizing a second stream of information into the first frame structure (Organizing DS-1s per Fig 1-2 into VTs per Fig 1-7) and selecting a second arrangement of synchronization bits to be written in the header section of the second information stream (Pointers for the VTs are assigned to the headers per Figs 1-2, 1-7, and 1-9) as claimed in **Claim 12.**

Further comprising;
transmitting the second stream of information with the second arrangement of synchronization bits (It would be obvious to one of ordinary skill in the art at the time of the invention that output of the MUX or transmitter would have VTs or second information stream with pointers or synchronization bits per Fig 1-2) as claimed in **Claim 13.**

In which the second stream of information is organized into a plurality of n parallel data streams (The DS-1s or n parallel data streams are organized into VTs per Fig 1-7)
In which the selection of the second arrangements of synchronization bits include writing n arrangements of synchronization bits (n pointers per Figs 1-2, 1-7 and 1-9), one arrangement for each parallel data stream header sections (one pointer for each VT)
Further comprising; interleaving the n parallel data streams in to the second stream of information (The n DS-1s are n parallel data streams which are interleaved into VTs per Figs 1-2, 1-7, and 1-9) as claimed in **Claim 14**.

Further comprising; following the transmission of the second information stream (VTs per Fig 1-7 made up of DS-1s or second stream), receiving the second stream of information;
Selecting the second arrangement of synchronization bits (Pointers associated with VTs per Figs 1-2, 1-7, and 1-9); using the second arrangement of synchronization bits (Pointers per Figs 1-2, 1-7, and 1-9) , synchronizing the second information stream in to the first frame structure (Pointer per Figs 1-2, 1-7, and 1-9) as claimed in **Claim 15A.**

In which the reception of the first stream of information includes receiving the information in a protocol selected from the group consisting of datacom, telecom,fiber channel, SONET, SDH, and Gigabit Ethernet protocols (SONET per Title) as claimed in **Claim 15B.**

SONET 101 does not expressly call for: synchronization bits but teaches pointers.
It would be obvious to one of ordinary skill in the art at the time of the invention that the pointers of SONET perform the same function as synchronization bits as shown in Fig 1-9.

Claim Rejections - 35 USC § 103

6.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.0 Claims 19-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuta et al. (U.S. Patent No.: 5,600,648 dated 2/4/97).

Referring to Claim 19, Furuta teaches: A selectable frame synchronization structure transmission repeater (Fig 13 or frame synchronization structure associated with a SONET equipment per Fig 18 which acts as a repeater)

A repeater input port to accept a first stream of information including a first arrangement of synchronization bits (30a or 30b accept a first string per Fig 1)

Decoder having a first input connected to the repeater input port to receive the first stream of information (431 per Fig 5B is the decoder), The decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section (431 per Fig 5B reads the POINTER bits in the frame structure of Fig 13 in order to determine the location of data or containers)
The decoder having a second input for selecting the first arrangement of synchronization bits to be read (431 per Fig 5B has a second input)

In Addition:

In which the organization of the second information stream in the first frame structure includes the first frame structure having a header section with a plurality of M bits (The V1s or second information stream per Fig 15 are in the first frame structure of Fig 13 which has a header of m bits) in which the selection of the second arrangement of synchronization bits includes a selecting a number of bits in the range from zero to m bits (pointers for the V1s define how the V1s are synchronized in the frame and the number of bits varies depending on the number of pointer from zero to m bits) as claimed in **Claim 20.**

In which the decoder selection or the first arrangement of synchronization bits includes selecting the bit position of the synchronization bits in the header section (431 or the decoder selects the bit positions of the pointer in the header per Fig 5B) as claimed in **Claim 21**

In which the decoder selection of the first arrangement of synchronization bits includes selecting the content of each synchronization bit in the header section (431 per Fig 5B selects the value or content of the pointers in the header section in order for the invention to work) as claimed in **Claim 22.**

A deinterleaver circuit having an input to receive the first steam of information, the deinterleaver circuit deinterleaving the first stream of information into a plurality of n parallel data streams (It would be obvious to one of ordinary skill in the art at the time of the invention that the EQUIPMENT#A of Fig 18 has a decoder which deinterleaves a single Vc-m stream and inserts

VC-m which consist of n parallel data streams or V1s as shown in Fig 15 in order for the invention to work)
In which the decoder's first input includes a plurality of n inputs connected to the deinterleaver to receive the first stream of information in n parallel data streams (The EQUIPMENT#A which inherently has a decoder receives a plurality of VC-ms in parallel data streams per Fig 18) the decoder's selection of the first arrangement of synchronization bits includes selecting an arrangement of synchronization bits in each of the n parallel data streams to form a first frame structure including header and data sections in each data stream (Pointers are inserted into the SONET frame structure associated with the V1s or parallel streams per Figs 12-18) as claimed in **Claim 23.**

In which the decoder's selection of the first arrangement of overhead bits includes selecting independent arrangements of synchronization bits for each header section of the n parallel data streams (It would be obvious to one of ordinary skill in the art at the time of the invention that there are separate pointers associated with the V1s per Figs 12-18) as claimed in **Claim 24**.

In which the deinterleaver circuit deinterleaves the first stream of digital information into four parallel data streams (It would be obvious to one of ordinary skill in the art at the time of the invention that deinterleaver circuit would break the V1s in to N parallel data streams from the SONET frames based upon pointers per Fig s 12-18) as claimed in **Claim 25**

An encoder having an output to provide the second stream of information organized in the first frame structure with header sections (It would be obvious to one of ordinary skill in the art at the time of the invention that EQUIPMENT#A per Fig 18 has an encoder for organizing the header of the SONET frame structure by adding pointers associated with the V1s or second streams) The encoder having an input for selecting a second arrangement of synchronization bits to be written in the header section (Inputs or adds pointer or synchronization bits associated with the V1s per Fig s 12-18) and a repeater output connected to the encoder output to provide the second stream of information (It would be obvious to one of ordinary skill in the art at the time of the invention that the output of EQUIPMENT#A contains a repeater which outputs STM-n which consists of VC-m per Fig 18) as claimed in **Claim 26.**

In which the encoder organizes the second stream of information into a plurality of n parallel data streams (It would be obvious to one of ordinary skill in the art at the time of the invention that the EQUIPMENT#A has an encoder in order insert VC-m in order to create STM-n per Fig 18), and in which the encoder in which the encoder selection of the second arrangement of the synchronization bits includes selecting the synchronization bits to be written in the header sections of the n parallel data streams (The encoder inserts pointers into the SONET frame structure in the header which synchronize the location of the V1s per Figs 12-18); and further comprising:

An interleaver circuit having a plurality of n inputs connected to n encoder outputs (It would be obvious to one of ordinary skill in the art at the time of the invention that the EQUIPMENT#A has an interleaver in order to encode the n V1s into the SONET Frame per Figs 12-18), the

interleaver circuit interleaving the parallel data streams in to the second stream of information (The V1s are made up of n parallel data streams per Figs 12-18), the interleaver circuit having an output connected to the repeater output (It would be obvious to one of ordinary skill in the art at the time of the invention that EQUIPMENT#A has a repeater in order to INSERT VC0ms into the STM-n per Fig 18) as claimed in **Claim 27**

In which the repeater input receives the first information stream in a protocol selected from the group consisting of datacom, telecom, fiber channel, SONET, SDH and Gigabit Ethernet protocols (SDH per Abstract) as claimed in **Claim 28.**

Furuta does not expressly call for: repeater.

It would be obvious to one of ordinary skill in the art at the time of the invention that the SONET equipment of Furuta performs the repeater function as it inserts and drops STMs as shown in Fig 18.

Referring to Claim 29, Furuta teaches: A selectable frame synchronization structure communication system comprising: (Fig 13 or selectable frame structure synchronization communication system)

A transmitter (It would be obvious that there is a transmitter in each of the Equipement per Fig 18) having an output to provide a first stream of information in a first structure with a header including a first arrangement of synchronization bits (Fig 13 or selectable frame structure with pointers providing synchronization)

A repeater input port to accept a first stream of information (30a or 30b accept a first string per Fig 1)

Decoder having a first input connected to the repeater input port to receive the first stream of information (431 per Fig 5B is the decoder), The decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section (431 per Fig 5B reads the POINTER bits in the frame structure of Fig 13 in order to determine the location of data or containers)
The decoder having a second input for selecting the first arrangement of synchronization bits to be read (431 per Fig 5B has a second input)

In Addition:

In which the repeater further includes; an encoder having an output to provide a second stream of information organized in the first structure with a header section (It would be obvious to one of ordinary skill in the art at the time of the invention that EQUIPMENT#A per Fig 18 encodes pointers associated with the VC-ms or second stream into the SONET FRAME per Figs 12-18),

the encoder having an input for selecting a second arrangement of the synchronization bits to be written in the header section (EQUIPMENT#A inputs the pointers or synchronization bits associated with the VC-ms or second stream per Figs 12-18); and

A repeater output connected to the encoder output to provide the second stream of information (It would be obvious to one of ordinary skill in the art at the time of the invention that EQUIPMENT#A has an repeater and it encodes the VC-m information in to STM-n per Figs 12-18) as claimed in **Claim 30.**

A receiver having a input connected to the repeater output to accept the second stream of information (EQUIPMENT #A or receiver has multiple input streams to be inserted per Fig 18) the receiver reading the second arrangement of synchronization bits to organized the second information stream into the first frame structure (EQUIPMENT#A reads the arrangement of sync bits in the VC-M which are to be created into a STM-n per Fig 18 which are organized into the first frame structure as shown in Figs 13-15) as claimed **Claim 31**.

Furuta does not expressly call for: transmitter or repeater.

It would be obvious to one of ordinary skill in the art at the time of the invention that the SONET equipment of Furuta performs the transmitter and repeater function as it inserts and drops STMs as shown in Fig 18.

Conclusion

8.0 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W Wilson whose telephone number is 703/305-4102. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas Olms can be reached on (703) 305-4703. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

Robert W Wilson
Examiner
Art Unit 2661

RWW
July 30, 2003

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